UTILITY PATENT APPLICATION TRANSMITTAL

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First Inventor or Application Identifier	Youichi TOBITA
Title	MULTILAYERED WIRING SUBSTRATE

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

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1. ■ Fee Transmittal Form (e.g. PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. ■ Specification — Total Pages: 23
3. ■ Drawing(s) *(35 U.S.C. 113)* — Total Sheets: 11 (Formals)
4. ■ Oath or Declaration — Total Pages: 3
   a. ■ Newly executed (original)
   b. □ Copy from a prior application *(37 C.F.R. §1.63(d))* *(for continuation/divisional with box 15 completed)*
      i. □ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*
5. □ Incorporation By Reference *(usable if box 4B is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4B, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

6. □ Assignment Papers (cover sheet & document(s))
7. □ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* □ Power of Attorney
8. □ English Translation Document *(if applicable)*
9. ■ Information Disclosure Statement (IDS)/PTO-1449 ■ Copies of IDS Citations (1)
10. □ Preliminary Amendment
11. ■ White Advance Serial No. Postcard
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16. Amend the specification by inserting before the first line the sentence:
□ This application is a □ Continuation □ Division □ Continuation-in-part (CIP) of application Serial No. Filed on
□ This application claims priority of provisional application Serial No. Filed

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Respectfully Submitted,

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TITLE OF THE INVENTION

Multilayered Wiring Substrate

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a printed (wiring) substrate or board and, in particular, to a multilayered wiring substrate or board having a plurality of multilayered wiring layers. The invention involves a technique of improving the difference in propagation delay time (hereinafter also referred to simply as "delay time") between signals propagating along a plurality of wirings that form the respective wiring layers.

Description of the Background Art

Fig. 15 shows appearances of a conventional memory module 200P (i.e., its top plan view and side view). In Fig. 15, the illustration of detailed wiring is omitted.

Referring to Fig. 15, in the memory module 200P a plurality of (nine in the figure) DRAMs (Dynamic Random Access Memory) 51 are mounted on a conventional multilayered wiring substrate 100P. The substrate 100P is provided with a plurality of external terminals 60, through which sending and/or receiving of signals and supply of power are performed between the DRAMs 51 and an external system or external circuit (not shown).

Fig. 16 is a schematic longitudinal section of the multilayered wiring substrate 100P taken along the line A-A of Fig. 15. The substrate 100P has six multilayered wiring layers, and wirings that form their respective wiring layers are isolated by an insulating material 2, such as glass epoxy material. Specifically, signal wiring groups 31 and 32, each forming a signal wiring layer, are disposed on both surfaces (main surfaces) of the multilayered wiring substrate 100P, respectively. Signal wiring groups 33 and 34, each forming a signal wiring layer, and a ground wiring (layer) 35, and a power supply

wiring (layer) 36 are disposed inside the multilayered wiring substrate 100P. The signal wiring groups 31 to 34 are used for transferring, for example, an address signal relative to the operation of the DRAM 51. The ground wiring 35 and power supply wiring 36 are used for supplying a ground potential and a power supply potential to a ground terminal and a power supply terminal of the DRAM 51, respectively.

Fig. 17 is a schematic top plan view of a signal wiring layer formed from a signal wiring group 31, as an example of wiring layers. As shown in Fig. 17, the signal wiring group 31 is composed of *n* strip-like signal wirings 31a to 31n which transfer, for example, an address signal of the DRAM 51. The signal wirings 31a to 31n are disposed in this order, so as to be parallel with one another.

In general, the signal wirings that form the signal wiring groups 31 and 32 on the surface of the multilayered wiring substrate 100P, are composed of a copper foil having a thickness of about 20 μm, and a copper plating film that has a thickness of about 20 microns and is disposed on the copper foil surface. The signal wirings that form the signal wiring groups 33 and 34 in the multilayered wiring substrate 100P, are composed of a copper foil having a thickness of about 40 μm. The signal wirings that form the signal wiring groups 31 to 34 have a width of about 100 to 200 μm, and the wiring interval of a wiring pattern is about 100 to 200 μm. On the other hand, the ground wiring 35 and power supply wiring 36 are composed of a plane copper foil having a thickness of about 40 μm. The length of the signal wirings that form the signal wiring groups 31 to 34 is about the same as the lateral width of the memory module 200P (i.e., the dimension in right-to-left direction in Fig. 15), and it is usually about ten and several centimeters.

Fig. 18 is a schematic longitudinal section of the multilayered wiring substrate 100P or memory module 200P taken along the line B-B of Fig. 15. As shown in Fig. 18,

there is formed a through hole 40 extending through in the direction of thickness of the multilayered wiring substrate 100P. The through hole 40 has a diameter of about 250 μm, and is bored by means such as a drill. A conductive layer 41 having a thickness of about 20 μm is formed on the inner wall or side wall 40S of the through hole 40. The conductive layer 41 is formed at the same time that the signal wiring groups 31 and 32 on the surface of the multilayered wiring substrate 100P are formed by copper plating. Referring again to Fig. 17, through holes 40ab to 40mn are interposed among the signal wirings 31a to 31n.

The through hole 40 and conductive layer 41 establish a connection between predetermined layers selected from the wiring layers formed from the signal wiring groups 31 to 34, the ground wiring layer 35, and the power supply wiring layer 36. For instance, as shown in Fig. 18, the wiring layers made by the signal wiring groups 33 and 34, respectively, are connected to the wiring layer made by the signal wiring group 31. The pad of one signal wiring in the signal wiring group 31 is connected via a solder 52 to an external lead 51a of the DRAM 51. Thereby, the DRAM 51 is connected to the wiring layers made by the signal wiring groups 33 and 34, or to each signal wiring.

The timing that the DRAM 51 receives an address signal SA will be described by referring to Fig. 19, which illustrates timing charts of a clock signal CL and address signal SA. The DRAM 51 receives the address signal SA at a rise (or fall) t0 of the clock signal CL as a reference time. In order that the address signal SA is surely received and the internal circuit of the DRAM 51 is operated stably, a set up time T1 and hold time T2, each having a predetermined period of time, are provided before and after time t0. For achieving high speed and stable operation of the DRAM 51, it is preferable to provide a greater operation margin to the set up time T1 and to the hold time T2.

When a plurality of address signals SA are transferred on different wirings, it is

desirable that all the address signals SA propagate simultaneously on the multilayered wiring substrate 100P, and that the DRAM 51 receives them at the same time. By establishing this transfer condition, the above-mentioned margin can be set at a large value, and a high operational stability of the DRAM 51 is obtainable even at high speed operation.

However, the conventional memory module 200P has the following problems in signal propagation. Description will now be made by taking, as an example, a wiring layer made by the above-mentioned signal wiring group 31. The same is true for other wiring layers.

It is well known that when a plurality of wirings are disposed in close proximity, these wirings are capacitively coupled via the capacitance (or capacitor) component formed between the wirings. This condition will be described by referring to Fig. 20, which is a schematic longitudinal section of the multilayered wiring substrate 100P taken along the line CP-CP of Fig. 17. As shown in Fig. 20, all the signal wirings 31a to 31n can be schematically illustrated as being in a capacitive coupling in series via a capacitance (or capacitor) CSW between two adjacent signal wirings.

Likewise, when the through holes 40ab to 40mn are interposed among the signal wirings 31a to 31n, as shown in Fig. 17, all the signal wirings 31a to 31n and all the through holes 40ab to 40mn (specifically, all the conductive layers 41ab to 41mn) can be illustrated as shown in Fig. 21, which is a schematic longitudinal section taken along the line DP-DP of Fig. 17. That is, all the signal wirings 31a to 31n and all the conductive layers 41ab to 41mn are capacitively coupled in series via a capacitance (or capacitor) CST between one signal wiring and the conductive layer of one through hole.

Referring again to Fig. 17, one signal wiring and one through hole are disposed on both sides of the signal wirings 31b to 31m except for the outermost signal wirings

31a and 31n. Whereas one signal wiring and one through hole are disposed only on one side of the outermost signal wirings 31a and 31n. Specifically, as shown in Figs. 20 and 21, two capacitance CSW or two capacitance CST are coupled to the signal wirings 31b to 31m, whereas only one capacitance CSW or capacitance CST is coupled to the outermost signal wirings 31a and 31n.

A propagation delay time per unit of length of wiring tpd is expressed by the following Equation (1):

$$tpd = \sqrt{(L \cdot C)} \qquad \cdots (1)$$

where L and C represent inductance and capacitance per unit of length of wiring, respectively.

Since the capacitance C contains the capacitance CST or CSW as described above, it can be seen from Equation (1) that a delay time tpd1 of the signal wiring 31a or 31n is smaller than a delay time tpd2 of any of other signal wirings 31b to 31m. Further, in view of the fact that Equation (1) is a relational expression of per unit of length of wiring, it can be seen that these delay time tpd1, tpd2, and a difference therebetween Δ tpd depend on the length of wiring, and their values increase as the length of wiring increases.

Referring to timing charts of Fig. 22, it can be seen that since the delay time tpd1 is shorter than the delay time tpd2, address signals SAa and SAn that propagate along the signal wirings 31a and 31n propagate faster than address signals SAb to SAm that propagate along the signal wirings 31b to 31m, by the amount of time Δt (corresponding to the value obtained by multiplying a delay time difference Δtpd by the length of a signal wiring). For obtaining a stable operation of the DRAM 51, it is necessary to set the operating timing of the DRAM 51 by taking into consideration a difference Δt in propagation delay time among the address signals SAa to SAn. That is,

a hold time T3 to the address signal SAa and SAn is required to be shorter than a hold time T2 to the address signals SAb to SAm, by the amount of time Δt. This time setting will narrow each margin to the set up time and hold time, thus lowering the stability of the DRAM 51 at high speed operation.

SUMMARY OF THE INVENTION

According to a first aspect of the invention, a multilayered wiring substrate comprising: a plurality of multilayered wiring layers, at least one of the multilayered wiring layers containing a signal wiring group made by a plurality of signal wirings disposed in parallel with one another; and dummy wirings disposed outside said signal group in parallel to the signal wirings, at least one of the dummy wirings being disposed at each side of the signal wiring group.

According to a second aspect, the multilayered wiring substrate of the first aspect further comprises: through holes formed in a stacking direction of the wiring layers and disposed in each clearance between the signal wirings; a dummy through hole extending in the stacking direction, disposed adjacent to the dummy wiring on the side on which the signal wiring group is present; and conductive layers disposed inside the through holes and the dummy through hole, respectively.

According to a third aspect, the multilayered wiring substrate of the second aspect is characterized in that the conductive layer in the dummy through hole is electrically connected to the conductive layer in any one of the through holes.

According to a fourth aspect, the multilayered wiring substrate of the second aspect is characterized in that the conductive layer in the dummy through hole is electrically connected to the dummy wiring.

According to a fifth aspect, the multilayered wiring substrate of the first aspect further comprises at least one resistance having approximately the same impedance as a

characteristic impedance of the dummy wiring, and being electrically connected to an end or central part of the dummy wiring.

According to a sixth aspect, the multilayered wiring substrate of the first aspect further comprises at least one terminal for connecting a terminating resistance connected electrically to an end or central part of the dummy wiring.

In the first aspect, the line capacitance of the outermost signal wiring of the signal wiring group can be made equal to that of other signal wirings. Therefore, since the propagation velocity of signals can be made identical, the propagation delay time difference of the signals can be considerably reduced or eliminated. It is therefore able to operate a DRAM stably and reliably even at high speed operation, by taking, for example, such a construction that the multilayered wiring substrate is applied to a memory module and the access signal inputted to the DRAM is transferred by the respective signal wirings.

In the second aspect, the effect resulting from the first aspect can be further improved by the presence of the conductive layer in the dummy through hole.

In the third aspect, electrical influences, such as the field distribution of the conductive layer in the dummy through hole, can be made equal to that of the conductive layer in the through hole to which the conductive layer of the dummy through hole is electrically connected. Thereby, the electrical influence between the dummy through hole and through hole can be made equal to that of the signal wiring between other through holes. This more ensures the effect of the first aspect.

In the fourth aspect, the conductive layer of the dummy through hole is not directly connected to the conductive layer of the through hole, unlike the multilayered wiring substrate of the third aspect. Therefore, when the conductive layer of the through hole is electrically connected to the signal wiring, the conductive layer of the dummy

through hole does not serve as load of a signal that propagates along the signal wiring. As a result, the effect of the first aspect is obtained reliably while suppressing an increase in delay of the signal and in its waveform distortion.

In the fifth aspect, the dummy wiring is brought into an impedance matching by the resistance. When signal wirings are used in their impedance matching conditions, the electrical connecting condition of the dummy wiring can be made equal to that of the signal wirings. This more ensures the effect of the first aspect.

In the sixth aspect, since the terminating resistance connected electrically to a terminal for terminating resistance is disposed outside the multilayered wiring substrate, it is easy to set or change the resistance value of the terminating resistance. Hereat, in the above-mentioned memory module, a further reduction in power consumption is attainable, as compared to the case with the multilayered wiring substrate of the fifth aspect.

It is an object of the present invention to provide a multilayered wiring substrate capable of considerably reduce or eliminate the difference in propagation delay time between signals.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic top plan view of a wiring layer in a multilayered wiring substrate according to a first preferred embodiment of the invention;

Fig. 2 is a schematic view illustrating a capacitive coupling condition of a plurality of wirings in the multilayered wiring substrate according to the first preferred embodiment of the invention;

Fig. 3 is a schematic view illustrating a capacitive coupling condition of a plurality of wirings and conductive layers of through holes in the multilayered wiring substrate according to the first preferred embodiment of the invention;

Fig. 4 is a schematic view illustrating a dummy wiring in the multilayered wiring substrate according to the first preferred embodiment of the invention;

Fig. 5 is a schematic longitudinal section of a multilayered wiring substrate according to a first modification of the first preferred embodiment;

Fig. 6 is a schematic longitudinal section of a multilayered wiring substrate according to a second modification of the first preferred embodiment;

Fig. 7 is a schematic top plan view of a memory module according to a second preferred embodiment;

Fig. 8 is a schematic top plan view of a memory module according to a first modification of the second preferred embodiment;

Fig. 9 is a schematic top plan view of a memory module according to a second modification of the second preferred embodiment;

Fig. 10 is a schematic top plan view of other memory module according to the second modification of the second preferred embodiment;

Fig. 11 is a schematic top plan view of a memory module according to a third modification of the second preferred embodiment;

Fig. 12 is a schematic top plan view of another memory module according to the third modification of the second preferred embodiment;

Fig. 13 is a schematic top plan view of a memory module according to a fourth modification of the second preferred embodiment;

Fig. 14 is a schematic top plan view of another memory module according to the fourth modification of the second preferred embodiment;

Fig. 15 is a diagram of appearances of a memory module using a conventional multilayered wiring substrate;

Fig. 16 is a schematic longitudinal section of a conventional multilayered wiring substrate;

Fig. 17 is a schematic top plan view of a wiring layer in the conventional multilayered wiring substrate;

Fig. 18 is a schematic longitudinal section of the conventional multilayered wiring substrate;

Fig. 19 is a timing chart illustrating timing that a DRAM receives an address signal;

Fig. 20 is a schematic view illustrating a capacitive coupling condition of a plurality of wirings in the conventional multilayered wiring substrate;

Fig. 21 is a schematic view illustrating a capacitive coupling condition of a plurality of wirings and conductive layers of through holes in the conventional multilayered wiring substrate; and

Fig. 22 is a timing chart illustrating timing that a DRAM receives a plurality of address signals having a propagation delay time therebetween.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Preferred Embodiment

A multilayered wiring substrate 100 according to a first preferred embodiment comprises a plurality of signal wiring layers, a ground wiring (layer) 35, a power supply wiring (layer) 36, and a plurality of through holes formed in the stacking direction of these wiring layers, as in the conventional multilayered substrate 100P shown in Figs. 15 to 18. The wirings that form the respective wiring layers and signal wiring layers are isolated each other by an insulating material such as glass epoxy material (see the

insulating material 2 stated earlier). Description will now be made by taking, as an example, a signal wiring layer disposed on the surface of the multilayered wiring substrate 100. The same is true for other signal wiring layers. Fig. 1 is a schematic top plan view of the above-mentioned signal wiring layer.

Referring to Fig. 1, the multilayered wiring substrate 100 comprises: (I) a signal wiring group 31 made by *n* signal wirings 31a to 31n disposed in parallel one another; and (II) dummy wirings 31Da and 31Dn disposed on the outside of the signal wiring group 31, namely, on the side opposite from signal wirings 31b to 31m with respect to the outermost signal wirings 31a and 31n of the signal wiring layer 31, respectively. The dummy wirings 31Da and 31Dn extend in parallel with the signal wirings 31a to 31n. The dummy wirings 31Da and 31Dn have the same shape as the signal wirings 31a to 31n, and are disposed outside the signal wirings 31a and 31n, respectively, at the same intervals as that in the signal wirings 31a to 31n.

The multilayered wiring substrate 100 further comprises: (i) through holes 40ab to 40mn, as previously described, which are formed in the corresponding clearance among the signal wirings 31a to 31n; and (ii) dummy through holes 40Da and 40Dn having the same shape as the through holes 40ab to 40mn, which are formed in the clearance between the dummy wiring 31Da and signal wiring 31a, and between the dummy wiring 31Dn and signal wiring 31n, respectively. As stated above, conductive layers 41ab to 41mn (see Fig. 2 as will hereafter be described) are formed on the inner wall of the through holes 40ab to 40mn, respectively. The conductive layers 41ab to 41mn establish an electrical connection between predetermined wiring layers selected from the above-mentioned wiring layers. Conductive layer (or dummy conductive layer) 41Da and 41Dn (see Fig. 2) which are identical with the conductive layers 41ab to 41mn are formed on the inner wall of the dummy through holes 40Da and 40Dn, respectively.

The conductive layers 41ab to 41mn, 41Da, and 41Dn may be formed so as to completely fill the through holes 40ab to 40mn, 40Da, and 40Dn.

The signal wirings 31b to 31m, through holes 40ab to 40mn, and conductive layers 41ab to 41mn are called "normal signal wirings 31b to 31m," "normal through holes 40ab to 40mn" and "normal conductive layers 41ab to 41mn" against the dummy wirings 31Da and 31Dn, dummy through holes 40Da and 40Dn, and dummy conductive layers 41Da and 41Dn.

Fig. 2 is a schematic longitudinal section of the multilayered wiring substrate 100 taken along the line C-C of Fig. 1, and Fig. 3 is that taken along the line D-D of Fig. 1. Referring to Fig. 2, in the vicinity of the line C-C of Fig. 1, the signal wirings 31a to 31n and dummy wirings 31Da and 31Dn are capacitively coupled in series via a capacitance CSW between two adjacent wirings. Referring to Fig. 3, in the vicinity of the line D-D of Fig. 1, the signal wirings 31a to 31n and the dummy wirings 31Da and 31Dn, and the conductive layers 41ab to 41mn of the through holes 40ab to 40mn and the conductive layers 41Da and 41Dn of the dummy through holes 40Da and 40Dn, are capacitively coupled in series via a capacitance CST between one wiring and one conductive layer.

As shown by a comparison of Figs. 2 and 3 with Figs. 20 and 21, in the multilayered wiring substrate 100, two capacitance CSW or CST can be coupled to the outermost signal wirings 31a and 31n of the signal wiring group 31 by the presence of the dummy wirings 31Da and 31Dn, as in the case of the signal wirings 31b to 31m. Specifically, the line capacitance of the outermost signal wirings 31a and 31n can be made equal to that of the signal wirings 31a to 31n.

Thereby, the propagation velocity of all signals propagating along the signal wirings 31a to 31n, for example, address signals to be inputted to the DRAMs 51 (see

Figs. 15 and 18), can be made equal. Accordingly, the propagation delay time difference Δtpd between the address signals can be considerably reduced, as compared to the conventional multilayered wiring substrate 100P.

As a result, in a memory module using the multilayered wiring substrate 100 instead of the conventional multilayered wiring substrate 100P, the set up time and the hold time can be set a same value respectively among all the signal wirings 31a to 31n. This allows the DRAM 51 to operate stably and reliably even at high speed operation.

In view of the fact that the capacitance CSW or CST depends on the field distribution among wirings or among wirings and the conductive layers of through holes, and that the field exists in all directions from the wiring surface that is a conductor, it is more preferable to provide more dummy wirings 31Da1, 31Da2, ... on further outside from the dummy wiring 31Da (and dummy wiring 31Dn), as illustrated by the schematic longitudinal section in Fig. 4. Of course, these dummy wirings 31Da, 31Da1, 31Da2, ... have the same size as the signal wirings 31a to 31n, and are disposed at the same intervals as that in the signal wirings 31a to 31n. It is desirable to provide dummy through holes at the clearances among the dummy wirings 31Da, 31Da1, 31Da2, ... respectively, that is, adjacent to the dummy wirings 31Da, 31Da1, 31Da2, ... on the side of the signal wiring group 31, respectively. This enables to provide more uniform electrical influence, such as field distribution, on all the signal wirings 31a to 31n, thus enhancing the above-mentioned effect of reducing the delay time difference Δtpd. The number of dummy wirings is set based on the number of signal wirings and the shape and size of the multilayered wiring substrate 100.

First Modification of First Preferred Embodiment

In the case that the multilayered wiring substrate 100 includes a wiring layer having less number of wirings than other wiring layers and having no dummy wiring, the

following construction is adaptable. As shown in Fig. 5 which is a schematic longitudinal section of the multilayered wiring substrate 100, in the case that there is a signal wiring layer including an outermost signal wiring 131a under a signal wiring 31b and no signal wirings under a signal wiring 31a, a conductive layer 41Da of a dummy through hole 40Da may be electrically connected to a normal conductive layer 41ab by a connecting wiring 43. The connecting wiring 43 is preferably provided within the signal wiring layer including the signal wiring 131a.

With this construction, the electrical influence such as the potential of the conductive layer 41Da of the dummy through hole 40Da and the field distribution can be made equal to that in the normal conductive layer 41ab. Therefore, the electrical influence of the signal wiring 31a disposed between the normal through hole 40ab and dummy through hole 40Da can be made the same as in the signal wirings disposed between other normal through holes. As a result, the above-mentioned propagation delay time difference Δtpd can be more reduced.

Although the foregoing description is directed to the case that the dummy conductive layer 41Da is connected to the adjacent normal conductive layer 41ab, the dummy conductive layer 41Da may be electrically connected to the conductive layer of other through hole that is not shown in Fig. 5. In addition, the normal conductive layer 41ab or the like, to which the dummy conductive layer 41Da is connected, may be electrically connected to the ground wiring 35 or power supply wiring 36.

Second Modification of First Preferred Embodiment

In the multilayered wiring substrate 100 according to the first modification, there is a case that the conductive layer 41Da of the dummy through hole 40Da may act as load of a signal propagating along the signal wiring 131a. This might increase the delay and waveform distortion of the signal. The increased delay can be reduced or

eliminated by a multilayered wiring substrate 100 having the construction according to a second modification. Fig. 6 is a schematic longitudinal section of a multilayered wiring substrate 100 according to the second modification. As shown in Fig. 6, a dummy wiring 131Da corresponding to the dummy wiring 31Da is disposed outside a signal wiring 131a, and the dummy wiring 131Da and a conductive layer 41Da of a dummy through hole 40Da are electrically connected via a connecting wiring 44.

With this construction, the increased delay in the signal can be suppressed because the dummy conductive layer 41Da is not directly connected to the normal conductive layer 41ab. In this case, the dummy wiring 131Da is preferably provided in a signal wiring layer including the signal wiring 131a. Of course, the dummy wiring 131Da offers the above-mentioned effect of reducing the delay time difference Δtpd.

Second Preferred Embodiment

A memory module 201 to which a multilayered wiring substrate 100 is applied will be described by referring to Fig. 7, which is a schematic top plan view of the memory module 201. To avoid confusion, only a signal wiring 31a and dummy wiring 31Da of the above-mentioned wirings are schematically illustrated in Fig. 7. The following description of the signal wiring 31a and dummy wiring 31Da is true for signal wirings 31b to 31n and the dummy wiring 31Dn. Since the construction of the DRAM 51, etc. is the same as that of the conventional memory module 200P, its illustration is omitted in Fig. 7. The same is true for Figs. 8 to 14 as will hereafter be described. The memory module 201 is of the type, e.g., RIMM (Rambus Inline Memory Module), in which an address signal is inputted from an (external) terminal T31a1 of the input side of the module 201 and the inputted address signal is not only transferred to a DRAM but also outputted from an (external) terminal T31a2 on the output side.

Referring to Fig. 7, in the memory module 201 the end part 31aT1 on the input

side of the signal wiring 31a is electrically connected to an external circuit or a driver circuit 300 via the terminal T31a1 on the input side of the memory module 201. The driver circuit 300 has approximately the same output impedance value R as the characteristic impedance Z0 of the signal wiring 31a. The end part 31aT2 on the output side of the signal wiring 31a is electrically connected to the terminal T31a2 on the output side of the memory module 201, and the terminal T31a2 is electrically connected via a resistance R31a to a ground wiring 35 (see Fig. 16) for terminating. The resistance R31a is a terminating resistance having approximately the same impedance value as the characteristic impedance Z0 of the signal wiring 31a. The terminal T31a2 may be electrically connected via the resistance R31a to the power supply wiring 36 (see Fig. 16). The same is true for the following description. Thus, the signal wiring 31a transfers address signals in its impedance matching state at both end parts 31aT1 and 31aT2 on the input and output sides, respectively.

The multilayered wiring substrate 101 applied to the memory module 201 further comprises a resistance R31Da1 disposed on the above-mentioned multilayered wiring substrate 100. Specifically, both end parts 31DaT1 and 31DaT2 on the input and output sides of the dummy wiring 31Da, respectively, are grounded via a resistance R31Da1. For the sake of convenience, the end parts on the input and output sides of the dummy wiring 31Da correspond to the end parts of the input and output sides of the signal wiring 31a, respectively. The resistance R31Da1 has approximately the same impedance value as the characteristic impedance Z0 (being equal to that of the signal wiring 31a) of the dummy wiring 31Da, and the dummy wiring 31Da is in its impedance matching condition, at both end parts 31DaT1 and 31DaT2. The resistance R31Da1 is made by a chip resistance, and it is mounted on the surface of the multilayered wiring substrate 101 and connected by soldering between the dummy wiring 31Da and ground

wiring 35.

Thus, in accordance with the multilayered wiring substrate 101 and memory module 201, the electrically connected condition of the dummy wiring 31Da can be made equal to that of the signal wiring 31a. This ensures the above-mentioned effect of reducing the propagation delay time difference Δ tpd, thereby making high speed operation of the DRAM 51 stable and reliable. Modifications of the multilayered wiring substrate 101 and memory module 201 will be described as below. The same effect is also obtainable with any construction of first to fourth modifications.

First Modification of Second Preferred Embodiment

Fig. 8 is a schematic top plan view of a memory module 202 according to a first modification of the second preferred embodiment. As shown by comparison of Fig. 8 with Fig. 7, in a multilayered wiring substrate 102 applied to the memory module 202, end parts 31DaT1 and 31DaT2 on the input and output sides of a dummy wiring 31Da are electrically connected to a terminal (terminal for connecting terminating resistance) T31Da1 on the input side and a terminal (terminal for connecting terminating resistance) T31Da2 on the output side of the memory module 202, respectively. The terminals T31Da1 and T31Da2 are grounded via a terminating resistance R31Da2 provided outside the memory module 202.

Thus, in the multilayered wiring substrate 102 and memory module 202, the resistance R31Da is provided outside the multilayered wiring substrate 102. It is therefore easy to set or change the resistance value of the resistance R31Da. At this time, depending on selection or setting of the resistance R31Da, a further reduction in power consumption is attainable as compared with the memory module 201. Of course, a resistance which has approximately the same impedance as the characteristic impedance Z0 previously described can be used as a resistance R31Da2.

Second Modification of Second Preferred Embodiment

Fig. 9 is a schematic top plan view of a memory module 203 according to a second preferred embodiment of the second preferred embodiment. The memory module 203 is of the type, e.g., DIMM (Double Inline Memory Module), in which an address signal is inputted via a terminal T31a1 on the input side of the module 203 from an end part 31aT1 on the input side of a signal wiring 31a and then transferred to a DRAM and an end part 31aT2 on the output side of the signal wiring 31a is not terminated. Specifically, a comparison of Fig. 9 with Fig. 7 indicates that in the memory module 203 the resistance R31a is not connected to the end part 31aT2 on the output side of the signal wiring 31a.

Correspondingly, in a multilayered wiring substrate 103 applied to the memory module 203, a terminating resistance R31Da1 is electrically connected only to an end part 31DaT1 on the input side of a dummy wiring 31Da. The end parts 31aT2 on the output side of the dummy wiring 31Da may be terminated at a resistance R31Da1 or R31Da2.

Like a multilayered wiring substrate 104 of a memory module 204 as shown in Fig. 10, an end part 31DaT1 on the input side of a dummy wiring 31Da may be electrically connected to a terminal T31Da1 on the input side, and the resistance R31Da2 may be connected to the terminal T31Da1. Again, an end part 31aT2 on the output side of the dummy wiring 31Da may be terminated at the resistance R31Da1 or R31Da2.

Third Modification of Second Preferred Embodiment

Fig. 11 is a schematic top plan view of a memory module 205 according to a third modification of the second preferred embodiment. The memory module 205 is of the type, e.g., DIMM type memory module, in which an address signal is inputted from a central part 31aC of a signal wiring 31a and transferred to a DRAM. This type memory module is often used for reducing by half the propagation delay time tpd of an address

signal on the memory module.

Referring to Fig. 11, in the memory module 205 a driver circuit 300 is electrically connected via an (external) terminal T31a3 to the central part 31aC of the signal wiring 31a in the direction of length of the signal wiring 31a. Correspondingly, in a multilayered wiring substrate 105 applied to the memory module 205, a resistance R31Da1 is electrically connected to a central part 31DaC of the signal wiring 31Da in the direction of length of a dummy wiring 31Da.

Like a multilayered wiring substrate 106 of a memory module 206 shown in Fig. 12, the central part 31DaC of the dummy wiring 31Da may be electrically connected to a terminal (terminal for connecting terminating resistance) T31Da3, and a resistance R31Da2 may be electrically connected to a terminal T31Da3.

Fourth Modification of Second Preferred Embodiment

Fig. 13 is a schematic top plan view of a memory module 207 according to a fourth modification of the second preferred embodiment. As shown by comparison of Fig. 13 with Fig. 11, in the memory module 207, end parts 31aT1 and 31aT2 of a signal wiring 31a is electrically connected to terminals T31a1 and T31a2 and then grounded via resistances R31a, respectively. Correspondingly, in a multilayered wiring substrate 107 applied to the memory module 207, the above-mentioned resistance R31Da1 is electrically connected to end parts 31DaT1 and 31DaT2 of a dummy wiring 31Da, respectively, in addition to a central part 31DaC.

Like a multilayered wiring substrate 108 of a memory module 208 as shown in Fig. 14, end parts 31DaT1 and 31DaT2 and a central part 31DaC of a dummy wiring 31Da may be electrically connected to terminals T31Da1, T31Da2 and T31Da3, respectively, and the resistance R31Da2 may be electrically connected to the terminal T31Da1, T31Da2 and T31Da3, respectively.

In the foregoing first to fourth modifications, when two or more of resistance R31Da1 or R31Da2 are electrically connected to a dummy wiring 31Da, any connecting conditions in various combinations are adaptable. For example, the end part 31DaT1 is electrically connected to the resistance R31Da1, and the end part 31DaT2 is electrically connected via the terminal T31Da2 to the resistance R31Da2.

Furthermore, a variable resistance may be used as resistances R31Da1, R31Da2 and R31Da3. The resistances R31Da1, R31Da2 and R31Da3 may be electrically connected to a ground wiring or power supply wiring of the memory modules 201 to 208. Of course, the signal wirings 31a to 31n are adaptable as a variety of data input/output lines for transferring signals other than address signals.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

WHAT IS CLAIMED IS:

1. A multilayered wiring substrate, comprising:

a plurality of multilayered wiring layers, at least one of said multilayered wiring layers containing a signal wiring group made by a plurality of signal wirings disposed in parallel with one another; and

dummy wirings disposed outside said signal wiring group in parallel to said signal wirings, at least one of said dummy wirings being disposed at each side of said signal wiring group.

2. The multilayered wiring substrate according to claim 1, further comprising:

through holes formed in a stacking direction of said wiring layers and disposed in each clearance between said signal wirings;

a dummy through hole extending in said stacking direction, disposed adjacent to said dummy wiring on the side on which said signal wiring group is present; and

conductive layers disposed inside said through holes and said dummy through hole, respectively.

3. The multilayered wiring substrate according to claim 2 wherein

said conductive layer in said dummy through hole is electrically connected to said conductive layer in any one of said through holes.

4. The multilayered wiring substrate according to claim 2 wherein

said conductive layer in said dummy through hole is electrically connected to said dummy wiring.

5. The multilayered wiring substrate according to claim 1, further comprising at least one resistance having approximately the same impedance as a characteristic impedance of said dummy wiring, and being electrically connected to an end or central part of said dummy wiring.

6. The multilayered wiring substrate according to claim 1, further comprising at least one terminal for connecting a terminating resistance connected electrically to an end or central part of said dummy wiring.

ABSTRACT OF THE DISCLOSURE

Each wiring layer of a multilayered wiring substrate (100) comprises signal wirings (31a to 31n) disposed in parallel with one another, and dummy wirings (31Da, 31Dn) disposed at each side of the signal wiring group (31) made by signal wirings (31b to 31m), respectively. The dummy wirings (31Da, 31Dn) have the same shape as the signal wirings (31a to 31n), and are disposed in parallel to the signal wirings (31b to 31m) at the same intervals as that in the signal wirings (31a to 31n). Through holes (40ab to 40mn) are formed in the respective clearances among the signal wirings (31a to 31n). Dummy through holes (40Da, 40Dn) having the same shape as the through holes (40ab to 40mn) are formed between the dummy wiring (31Da, 31Dn) and signal wiring (31a, 31n). A conductive layer is formed on the inner wall of the through holes (40ab to 40mn, 40Da, 40Dn). With the multilayered wiring substrate (100), it is able to reduce or eliminate the delay time difference between signals that propagate along the signal wirings.

FIG. 1

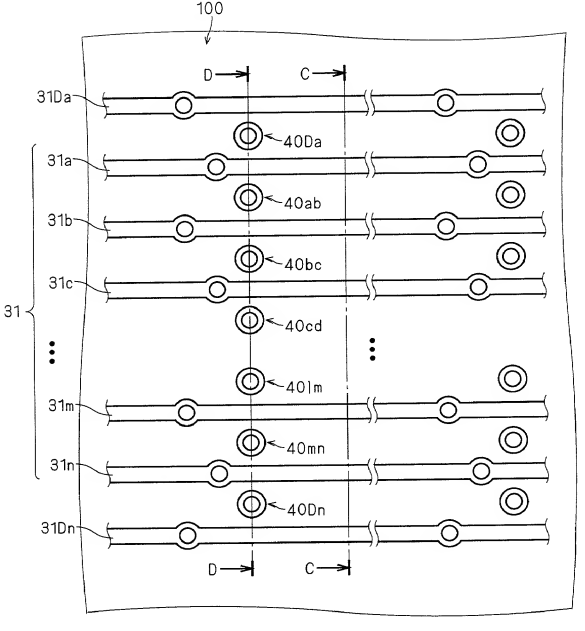

100
D
C
31Da
40Da
31a
40ab
31b
40bc
31c
31
40cd
40lm
31m
40mn
31n
40Dn
31Dn
D
C

FIG. 2

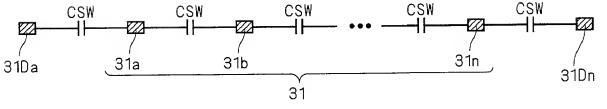


FIG. 3

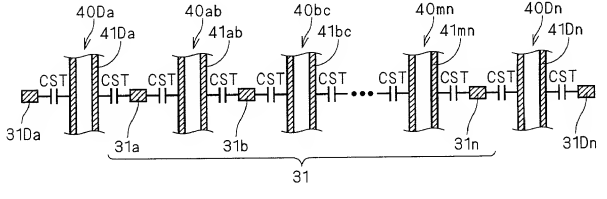


FIG. 4

FIG. 5

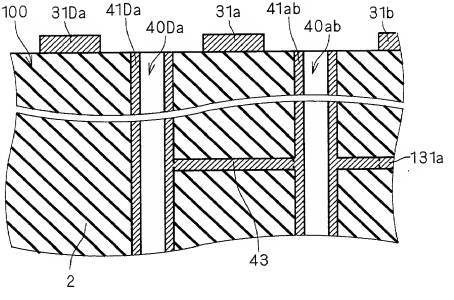


FIG. 6

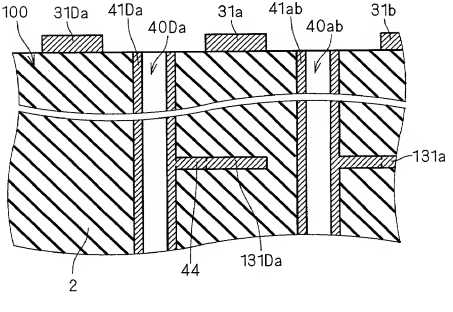


FIG. 7

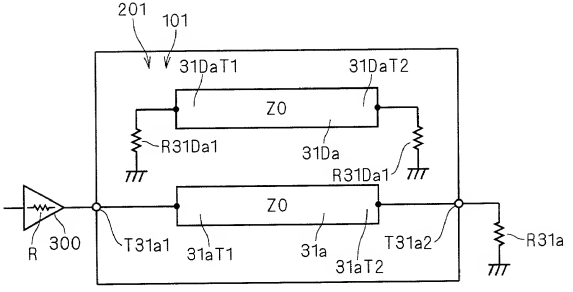

201
101
31DaT1
31DaT2
Z0
R31Da1
31Da
R31Da1
Z0
R
300
T31a1
31aT1
31a
T31a2
31aT2
R31a

FIG. 8

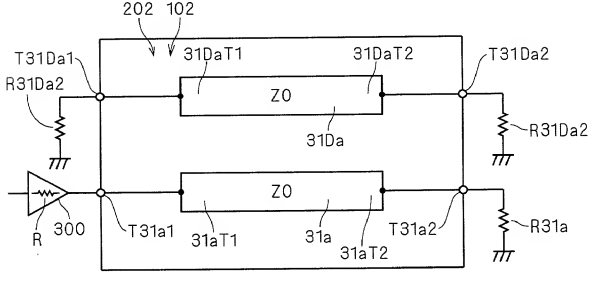

202
102
T31Da1
R31Da2
31DaT1
31DaT2
T31Da2
Z0
R31Da2
31Da
Z0
R
300
T31a1
31aT1
31a
T31a2
31aT2
R31a

FIG. 9

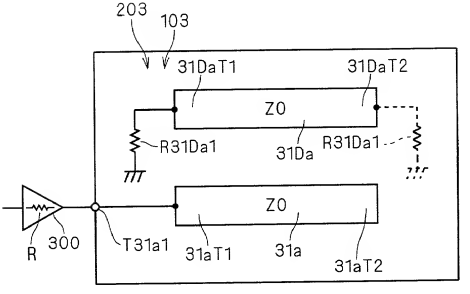

203
103
31DaT1
31DaT2
Z0
R31Da1
31Da
R31Da1
Z0
R
300
T31a1
31aT1
31a
31aT2

FIG. 10

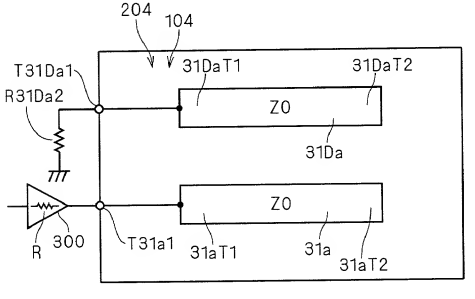

204
104
T31Da1
31DaT1
31DaT2
R31Da2
Z0
31Da
Z0
R
300
T31a1
31aT1
31a
31aT2

FIG. 11

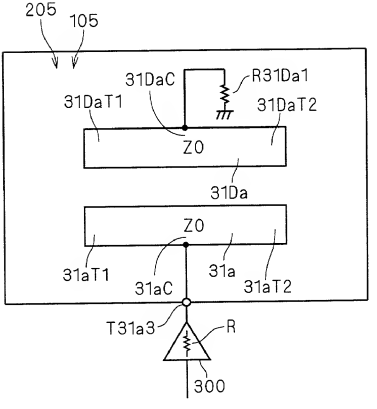
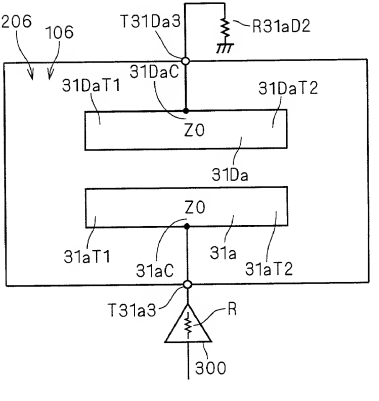

205
105
31DaC
R31Da1
31DaT1
31DaT2
Z0
31Da
Z0
31aT1
31aC
31a
31aT2
T31a3
R
300

FIG. 12


206
106
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R31aD2
31DaC
31DaT1
31DaT2
Z0
31Da
Z0
31aT1
31aC
31a
31aT2
T31a3
R
300

FIG. 13

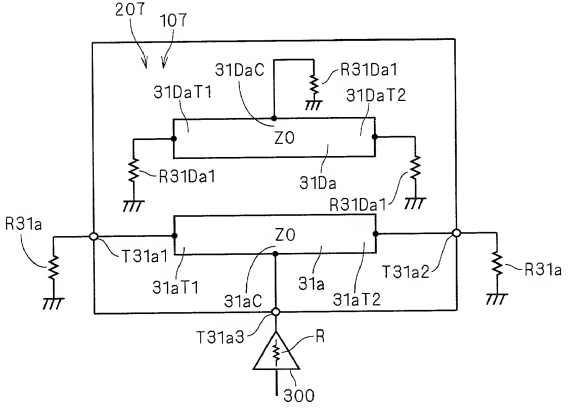

207
107
31DaC
R31Da1
31DaT1
31DaT2
Z0
R31Da1
31Da
R31Da1
R31a
Z0
T31a1
31aT1
31aC
31a
31aT2
T31a2
R31a
T31a3
R
300

FIG. 14

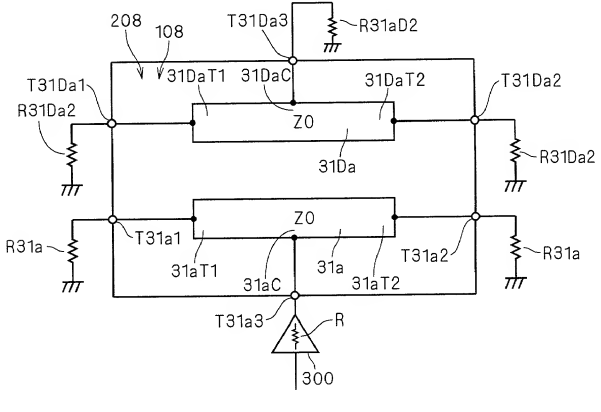

208
108
T31Da3
R31aD2
T31Da1
R31Da2
31DaT1
31DaC
31DaT2
T31Da2
Z0
31Da
R31Da2
Z0
R31a
T31a1
31aT1
31aC
31a
31aT2
T31a2
R31a
T31a3
R
300

FIG. 15

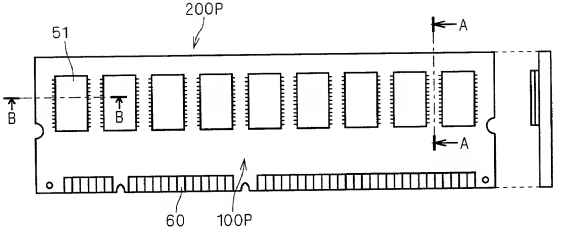


FIG. 16

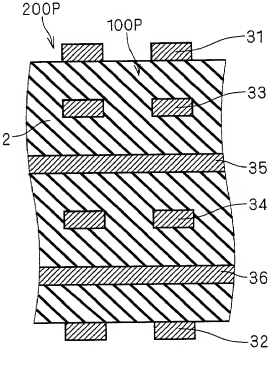


FIG. 17

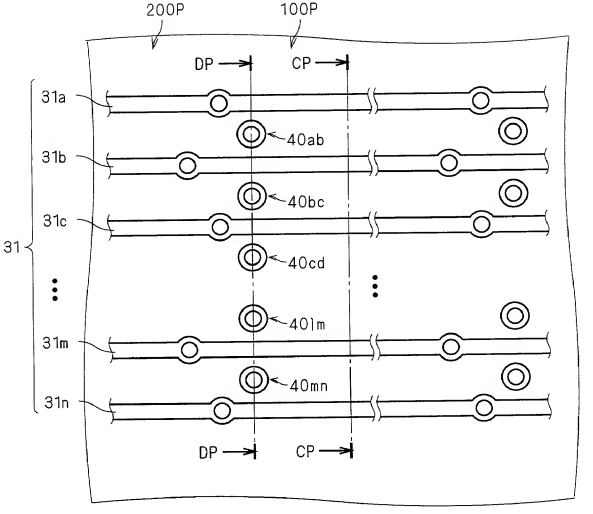

200P
100P
DP
CP
31a
31b
31c
31
31m
31n
40ab
40bc
40cd
401m
40mn
DP
CP

FIG. 18

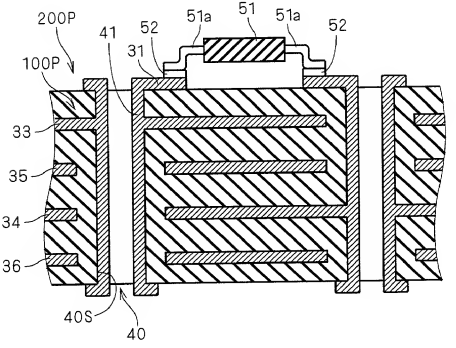

200P
41
52
51a
51
51a
52
31
100P
33
35
34
36
40S
40

FIG. 19

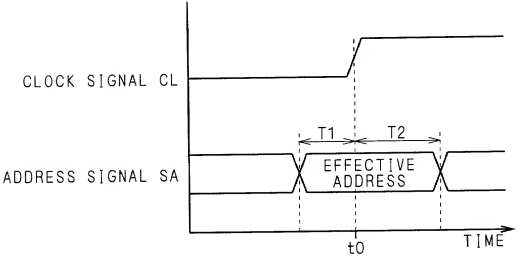

CLOCK SIGNAL CL
T1
T2
ADDRESS SIGNAL SA
EFFECTIVE ADDRESS
t0
TIME

FIG. 20

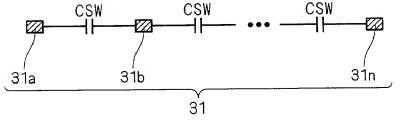


FIG. 21

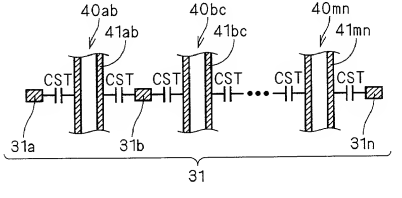
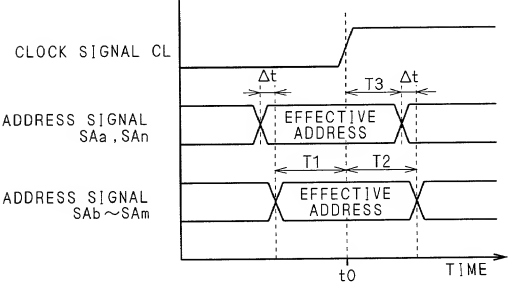


FIG. 22



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

MULTILAYERED WIRING SUBSTRATE

上記発明の明細書は、

- ☒ 本書に添付されています。
- ☐ ____月____日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、（該当する場合）_____に訂正されました。

the specification of which

- ☒ is attached hereto.
- ☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条 (a) - (d) 項又は365条 (b) 項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365 (a) 項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張	
P11-276488	Japan	September 29, 1999	☒ Yes はい	☐ No いいえ
			☐ Yes はい	☐ No いいえ

私は、第35編米国法典119条 (e) 項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
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